# Lab Report-2

# Aim:

#### To verify the truth table of half adder and full adder by using XOR and NAND gates respectively and analyse the working of half adder and full adder circuit with the help of LEDs in simulator 1 and verify the truth table only of half adder and full adder in simulator 2.

Theory:

Adders are digital circuits that carry out addition of numbers. Adders are a key component of arithmetic logic unit. Adders can be constructed for most of the numerical representations like Binary Coded Decimal (BDC), Excess – 3, Gray code, Binary etc. out of these, binary addition is the most frequently performed task by most common adders. Apart from addition, adders are also used in certain digital applications like table index calculation, address decoding etc.  
  
Binary addition is similar to that of decimal addition. Some basic binary additions are shown below.

0 0 1 1

+0 +1 +0 +0

0 1 1 (carry) 1 0

Schematic representation of half adder

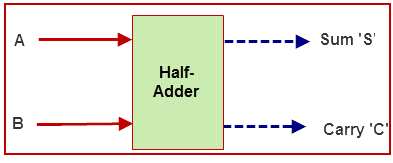
1. Half Adder

Half adder is a combinational circuit that perfoms simple addition of two binary numbers. The block diagram of a half adder is shown below

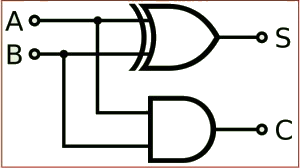
* 1. Half Adder Truth Table

If we assume A and B as the two bits whose addition is to be performed, a truth table for half adder with A, B as inputs and Sum, Carry as outputs can be tabulated as follows.

The sum output of the binary addition carried out above is similar to that of an Ex-OR operation while the carry output is similar to that of an AND operation. The same can be verified with help of Karnaugh Map.



If A and B are binary inputs to the half adder, then the logic function to calculate sum S is Ex – OR of A and B and logic function to calculate carry C is AND of A and B. Combining these two, the logical circuit to implement the combinational circuit of half adder is shown below.

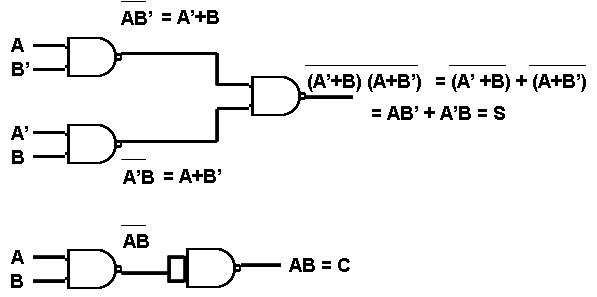


**Half Adder Logic Diagram**

As we know that NAND and NOR are called universal gates as any logic system can be implemented using these two, the half adder circuit can also be implemented using them. We know that a half adder circuit has one Ex – OR gate and one AND gate.

#### 1.2) Half Adder using NAND gates

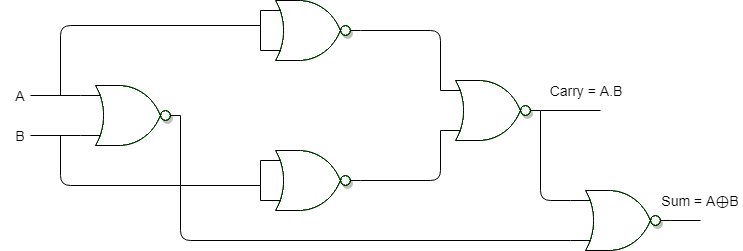
Five NAND gates are required in order to design a half adder. The circuit to realize half adder using NAND gates is shown below.



**Realization of half adder using NAND gates**

#### **1.3)** Half Adder using NOR gates

Five NOR gates are required in order to design a half adder. The circuit to realize half adder using NOR gates is shown below.

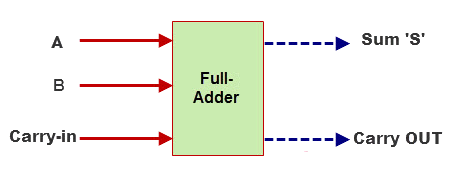


**Realization of half adder using NOR Gates**

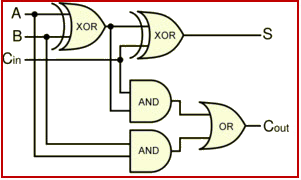
# 2.) Full Adder

Full adder is a digital circuit used to calculate the sum of three binary bits which is the main difference between full adder and half adder. Full adders are complex and difficult to implement when compared to half adders. Two of the three bits are same as before which are A, the augend bit and B, the addend bit. The additional third bit is carry bit from the previous stage and is called 'Carry' – in generally represented by CIN. It calculates the sum of three bits along with the carry. The output carry is called Carry – out and is represented by COUT.

The block diagram of a full adder with A, B and CIN as inputs and S, COUT as outputs is shown below.

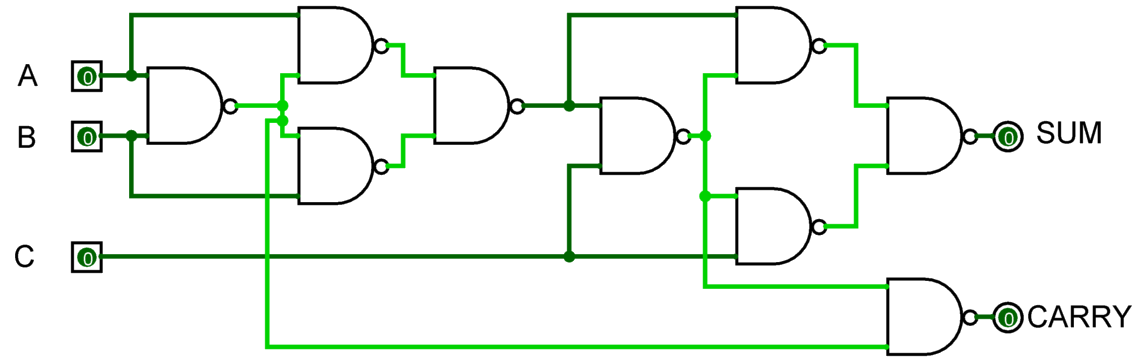
The simplified equation for sum is S = A'B'Cin + A'BCin' + ABCin  
The simplified equation for COUT is COUT = AB + ACIN + BCIN

In order to implement a combinational circuit for full adder, it is clear from the equations derived above, that we need four 3-input AND gates and one 4-input OR gates for Sum and three 2-input AND gates and one 3-input OR gate for Carry – out.



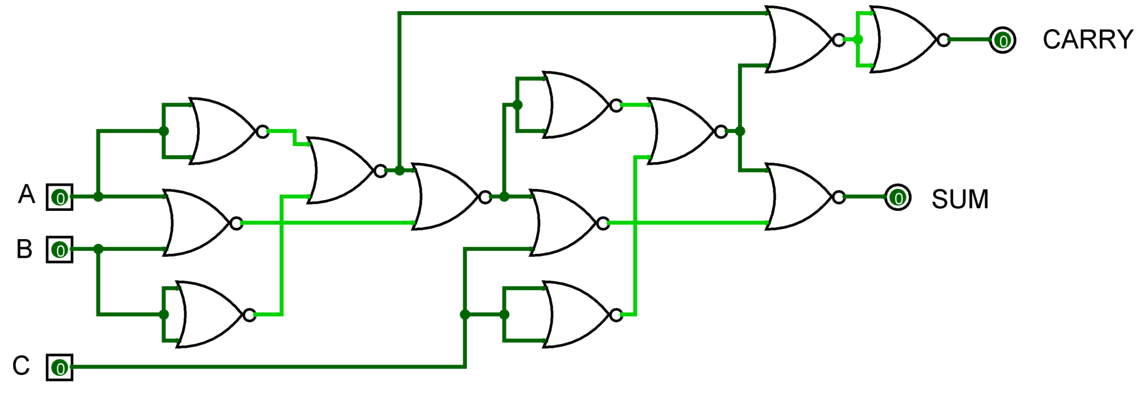
#### 2.1) Full Adder using NAND gates

As mentioned earlier, a NAND gate is one of the universal gates and can be used to implement any logic design. The circuit of full adder using only NAND gates is shown below.



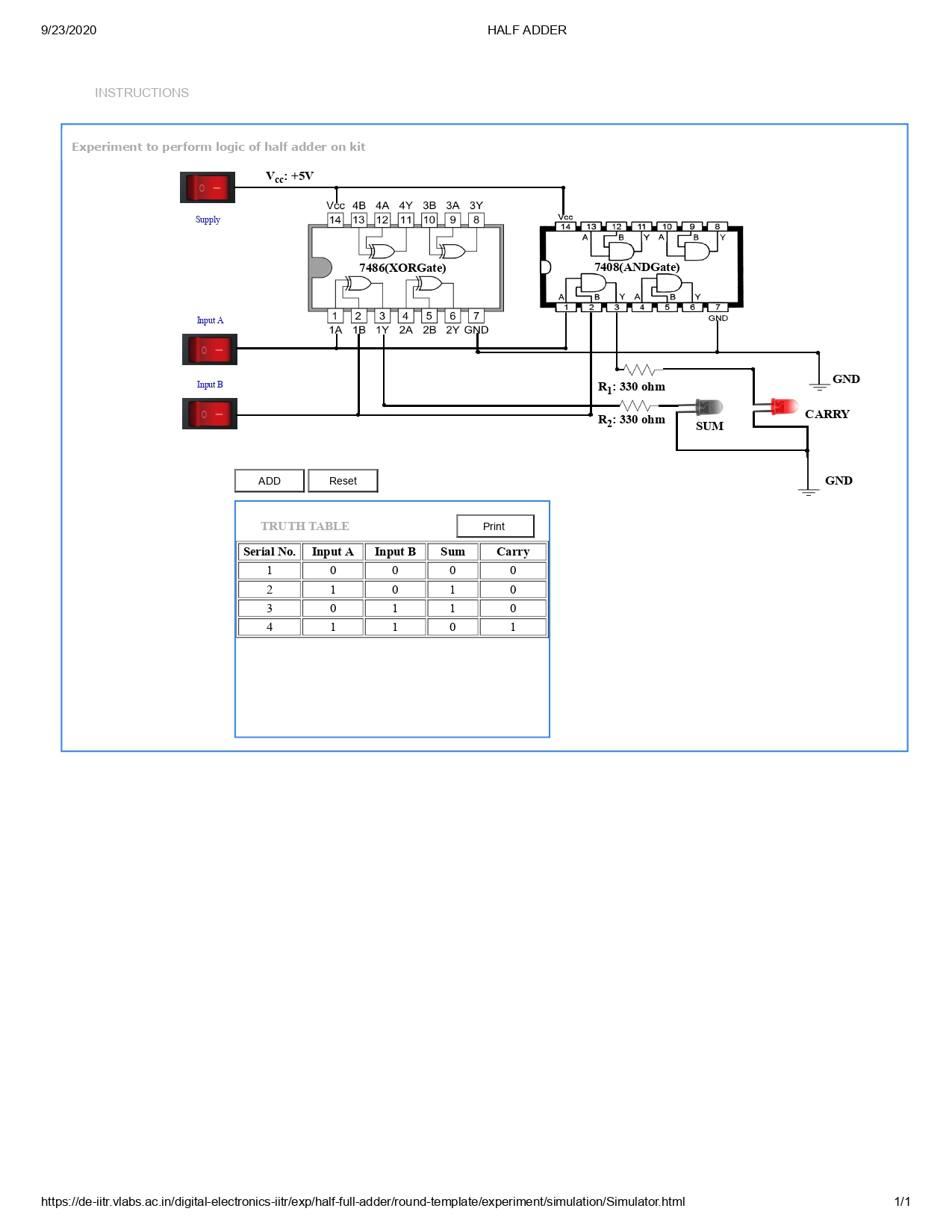
#### 2.2) Full Adder using NOR gates

#### As mentioned earlier, a NOR gate is one of the universal gates and can be used to implement any logic design. The circuit of full adder using only NOR gates is shown below.



**Full Adder using NOR gates**

**Conclusion:**

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